REMARKS

Amendments to the Specification

The misspelled acronym of "NOMS" is corrected in paragraph [19] to read "NMOS". No new matter is entered.

The drawings are objected to because the bypass capacitor connected to the second receiving terminal of the amplifier circuit as recited by claim 2 must be shown or the feature cancelled from the claim. It is noted that in lines 2-4 of claim 1 the first receiving terminal is defined as receiving the reference voltage and the second receiving terminal is defined as receiving the feedback voltage.

Applicant asserts that Fig.2 (and Fig.4) does already show the bypass capacitor Cp being connected to the second receiving terminal NA_2 of the amplifier circuit 32. As defined in claim 1 and as stated by the Examiner, the first receiving terminal NA_1 receives the reference voltage from the reference voltage generator 33, and the second receiving terminal NA_2 receives the feedback voltage from the feedback node NF_1. As shown in Fig.2 (and Fig.4), at least a bypass capacitor Cp is electrically connected to the second receiving terminal NA_2 of the amplifier circuit 32. Therefore, the bypass capacitor being connected to the second receiving terminal of the amplifier circuit as recited by claim 2 is already shown in original Fig.2 (and Fig.4). Reconsideration of the objection to the drawings in light of the above explanation is respectfully requested.

Claim 2 is objected to because in line 2 "second" should be –first – (see objection to the drawings above for reasoning). Appropriate correction is required.

Applicant asserts that there is in fact no error in the numbering of the receiving

terminal in claim 2. As described above in the response to the objection to the drawings, and as shown in Fig.2 (and Fig.4), at least a bypass capacitor Cp is electrically connected to the second receiving terminal NA_2 of the amplifier circuit 32. The numbering of the receiving terminals of claim 2 corresponds with the definition utilized in claim 1 and shown in the figures. Reconsideration of the objection to claim 2 in light of the above explanation is respectfully requested.

Claims 1, 3-15, and 17-24 are rejected under 35 USC 103a as being unpatentable over Smith (US 6,414,537) because the recitation of a series connection of two discharge transistors instead of a single discharge transistor 210 as utilized by Smith is not a patentable difference.

Applicant asserts that claims 1, 3-15, and 17-24 should not be found unpatentable over Smith because the utilizing two discharge transistors according to the present invention allows for a flexible and adjustable result in the transition of the disable mode, which is in contrast to the teachings of Smith.

According to the teachings of Smith as illustrated in Fig.2 and Fig.3 and the corresponding description, only one discharge transistor 210 is utilized. With only one discharge transistor 210, there is however possibility of mis-trigger of charging operation during discharging process. In the prior art Smith, while discharging, the voltage at terminal 208 is $V_R*R_2/(R_1+R_2)$. The feedback terminal 208 supplies the feedback voltage $V_R*R_2/(R_1+R_2)$ to the second input terminal of the amplifier 202. The amplifier 202 is a differential amplifier, which is controlled by the enable signal ENABLE. If the enable signal is "1", the amplifier 202 is enabled; while if the enable signal is "0", the amplifier 202 is disabled. In actual practice, the amplifier 202, however, would not be readily disabled when the enable signal becomes "0". That is, the amplifier 202 will be disabled only after a certain time delay. During the time delay, because the amplifier

202 is not immediately turned off by the enable signal, if the voltage at terminal 208, $V_R*R_2/(R_1+R_2)$, is substantially lower than the reference voltage V_{REF}, the amplifier 202 may function and may therefore output "a low driving voltage". This is because the voltage difference between the voltage at the first input terminal (the reference voltage V_{REF}) and the voltage at the second input terminal of the amplifier 202 (the feedback voltage) exceed a threshold set by the differential amplifier 202. If the amplifier 202 outputs "a low driving voltage", the transistor 204 will then be turned on. If the transistor 204 is turned on, the voltage regular circuit 200 will start to charge, which will affect the discharging process.

In the present invention, by utilizing two MOS transistors 41 and 42 respectively of an internal resistance r_{41} and r_{42}, a flexible and adjustable result in the transition of the disable mode is allowed. For example, by having adjustable sizes of the MOS transistors 41 and 42, while discharging from a loading capacitor CL, the voltage of the input of the amplifier circuit 32 (VNA_2) should be $r_{42}/(r_{42}+r_{41}) * V_{NOUT}$. By adjusting the size radio of two MOS transistors 41 and 42 (or adjusting the internal resistance r_{41} and r_{42} of the two MOS transistors), the voltage of the feedback terminal, which is the input of the amplifier, can be controlled not to make the amplifier 202 function when the amplifier 202 is not immediately turned off by the enable signal. In other words, the voltage of the feedback terminal is not substantially lower than the reference voltage V_{REF} and therefore the amplifier 202 does not function. The possible conflict of triggering charging operation during the discharging process is thereby prevented by utilizing two transistors 41, 42 according to the present invention. Therefore, the present invention provides a flexible and adjustable method in the transition of disable mode and improves the traditional voltage regulator by using two discharge transistors.

Reconsideration of independent claims 1 and 14 in light of the above explanation is respectfully requested. As claims 2-13 and 13-24 are dependent on claims 1 and 14, respectively, if claims 1 and 14 are found allowable, so too should the dependent claims 2-13 and 13-24. Further comments regarding the patentability of particular dependent

claims are provided below.

Claims 2 and 16 are rejected under 35 USC 103a as being unpatentable over Smith.

In the office action of 2006/1/25, the Examiner stated, "It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the voltage regulator circuit of Smith by utilizing a bypass capacitor in order to filter or bypass undesired frequency components as was old and known in the art at the time of the invention."

It is noted, however, that the Examiner did not find any prior art references that utilize a bypass capacitor Cp in the feedback path as is done in the present invention. Applicant asserts that this is due to that fact that it would not be obvious to utilize a bypass capacitor in the feedback path of a design having only a single discharge transistor 210 such as Smith because, as stated in paragraph [21] of the present invention, "If the bypass capacitor Cp is used in the prior art structure, the bypass capacitor Cp will induce serious side effect since it would lower the speed of voltage regulation of the second receiving terminal NA_2 and slow down the speed of disabling the prior art voltage regulator circuit 10."

This is in contrast to the present invention because the present invention includes two discharge transistors 41, 42. For example, as stated in paragraph [21] of the present invention, "Unlike the prior art, the feedback voltage in the voltage regulator circuit 30 according to the present invention shown in Fig. 2 can be quickly pulled down by the second discharge transistor 42, the speed of discharging and the efficiency of disabling are not sacrificed while employing the bypass capacitor Cp to suppress the noise. It allows the voltage regulator circuit 30 according to the present invention to output a low-noise, precise, and stable output voltage."

In conclusion, the bypass capacitor Cp of the present invention is placed at the

second input of the amplifier connecting to the loading module in the feedback path, which is an improvement over the prior art Smith in two aspects:

1. The bypass capacitor Cp can be quickly discharged through the two transistors 41, 42.

2. Using the bypass capacitor Cp combined with the resistant loading modules in the feedback path further reduces high frequency disturbance, especially when the voltage regulator circuit is implemented with devices operated at a high frequency.

Therefore, utilizing the combination of two discharge transistors 41, 42 and the bypass capacitor Cp allows the voltage regulator circuit 30 according to the present invention to output a low-noise, precise, and stable output voltage, and reduces high frequency disturbance. For at least the above reasons, applicant asserts claims 2 and 16 should not be found being unpatentable over Smith. Reconsideration of claims 2 and 16 is respectfully requested.

Sincerely yours,

/Winston Hsu/ Date: 05.09.2006

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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